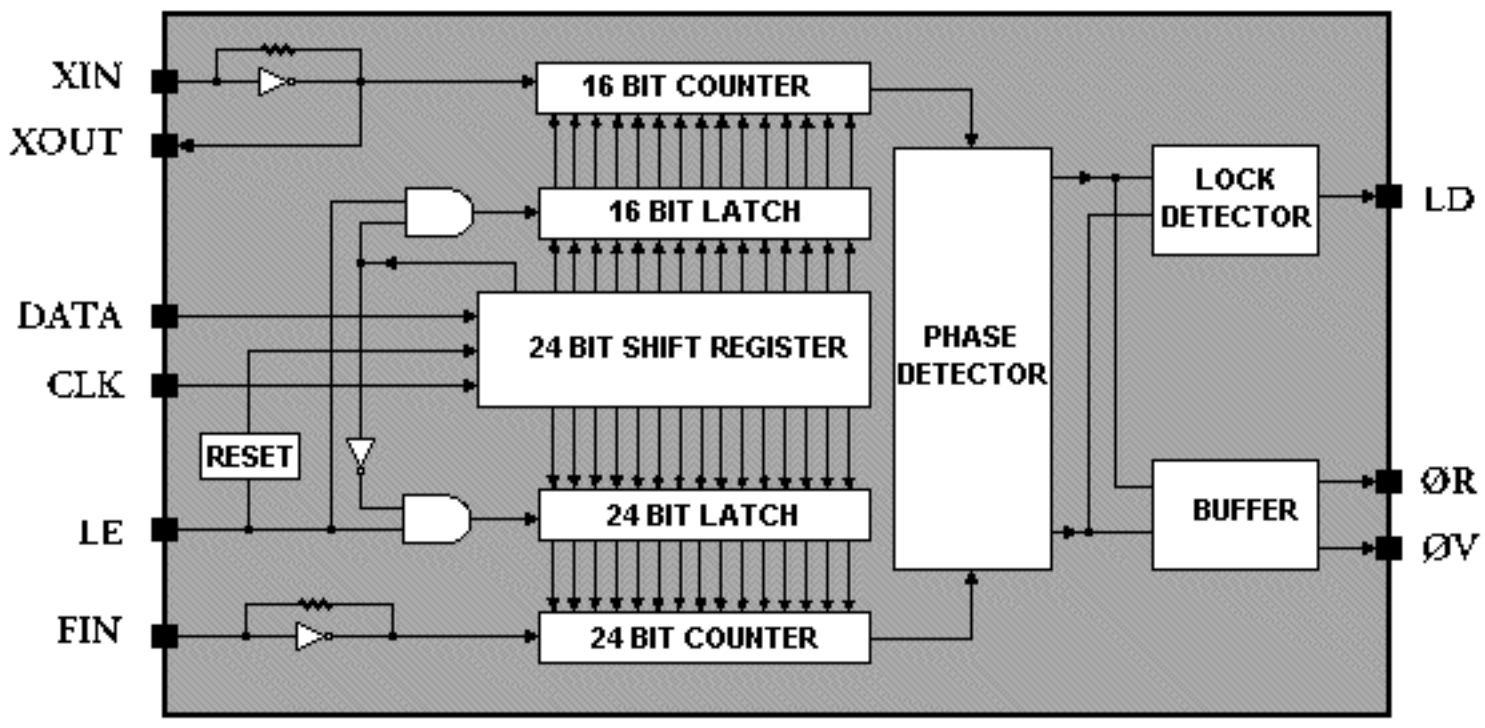
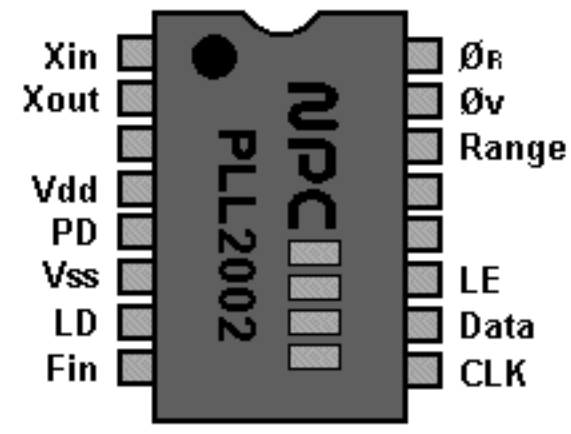
PLL2002

DESCRIPTION

The PLL2002A is a serial data programmable PLL Frequency Syntheseizer.
Ratios of reference frequency divider and input frequency divider can be independently set.



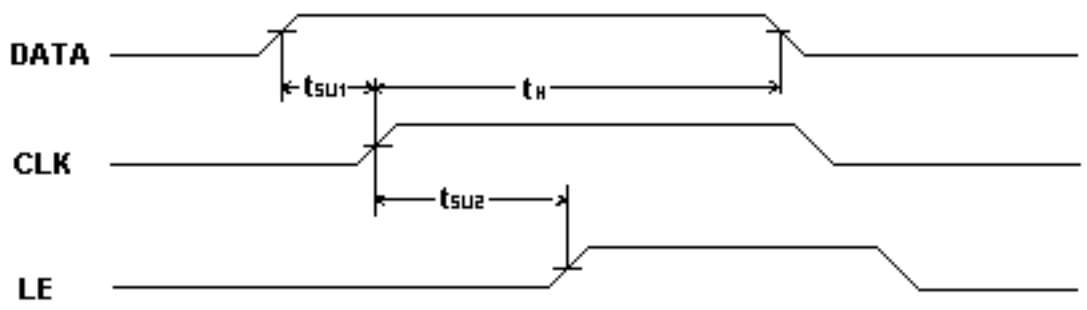


FEATURES

- Up to 550MHz input frequency (VDD=4.5V)
- Up to 20MHz reference frequency (VDD=4.5V)
- Up to 65535 programmable reference frequency divider ratio
- Up to 16777215 programmable input frequency divider ratio
- ϕ_V and ϕ_R output terminals
- Lock detector
- Either Active or Passive filter can be externally used.

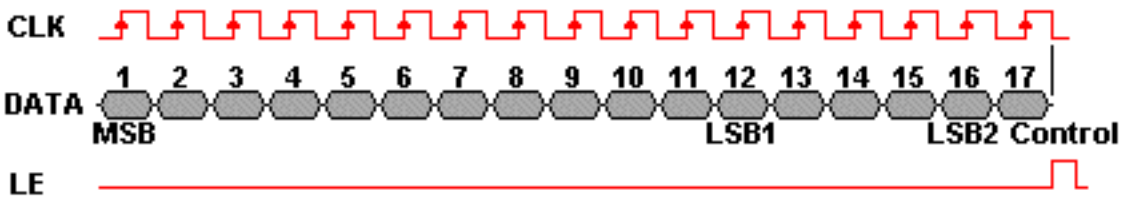
Pin	Name	Description
1	X_{IN}	Reference X-tal Oscillator Input
2	X_{OUT}	Reference X-tal Oscillator Output
3	NC	No Connection
4	V_{SS}	Positive Supply Voltage - 5 Volt
5	PD	Phase Detector Output - VCO Voltage Out
6	GND	Ground
7	LD	Loop Detector - Loop Detected=HIGH - Not Detected=LOW
8	F_{IN}	VCO Frequency In
9	CLK	Clock from CPU
10	Data	Data from CPU
11	LE	Latch Enable from CPU
12	NC	No Connection
13	NC	No Connection
14	Range	HIGH: F_{IN} is High Frequency Range. LOW: F_{IN} is Low Frequency Range
15	ϕ_V	Phase detector output to differential lowpass filter
16	ϕ_R	Phase detector output to differential lowpass filter

Serial data input timing



t_{su1} = 300nS
t_{su2} = 300nS
t_H = 300nS

Divider data setting procedure



Input data must be MSB first. Final bit is assigned to the control bit.
Data are written into shift register at the rising edge of the CLK signal.
When LE is HIGH, data is transferred from the shift register to either the latch of reference divider or input divider. Thus data must be written on the shift register while LE is remaining L0W.

While all bits of the N latch are "0", the N counter will be disabled.
While all bits of the R latch are "0", oscillator and R counter will be disabled.
While all bits of R and N latches are "0", both R and N counters will be disabled.

R packet is 16-bits MSB first hold the R Value, 1 Control Bit always signal that it is a R packet, then LE is toggled to complete this packet.

N packet is 24-bits, MSB first, the first 8 bits (In Range "LOW") are always low, the next 16 bits hold the N value, the a 0 control bit signals complete this packet.