ALIGNMENT OF P.L.L. PORTION 29XLR

1. Test equipment required

   a. Oscilloscope (0-50MHz)
   b. Frequency counter (0-50MHz)
   c. DC volt meter (10 volts maximum, 100K ohm/volt)

2. Alignment procedure

STEP	PRESET TO	CONNECTIONS	ADJUSTMENT	REMARKS
1	Channel 19	Oscilloscope to secondary of L5(TP1)	L5	Adjust L5 for the maximum indication on oscilloscope
2	Same as step 1	Frequency counter to secondary of L5(TP1)	VC1	Adjust VC1 to obtain 10.240 MHz indication
3	Same as step 1	DC volt meter to pin #5 of IC5(TP5)	L20	Adjust L20 to obtain approximately 3.0V reading
4	Same as step 1	Oscilloscope to secondary of L21(TP6)	L21	Adjust L21 for the maximum indication
5	Same as step 1	Frequency counter to secondary of L21(TP6)	L24	Adjust L24 to obtain 37.880 MHz indication

PLL Local Oscillator

Fvco, the output frequency of the VCO IC-5 is fed to one of the inputs of the PLL mixer, TR-18. Fstd, the output frequency of the local oscillator, TR-19, is 36.570 mhz, is fed to the other input of TR-18. These frequencies are mixed by TR-18 and the difference between Fvco and Fstd makes the input frequency to the programmable frequency divider.

The input frequency to the programmable divider Fl is calculated as follows:

$$Fl = Fvco - Fstd$$

Fl is fed to the programmable divider in the PLL IC, IC-3, through the interface gates in IC-4 and divided by N through the programmable divider. The frequency of 10.24 mhz is produced by the reference oscillator in IC-3 is divided by 1024 by the reference frequency divider in IC-3 and the resultant frequency, F2 is 10 khz.

$$F2 = 10.24 \text{ mhz} \div 1024 = 10 \text{ khz}$$

The output frequency of the programmable divider is compared with F2 at the phase detector in IC-3, in other words, these frequencies are phase detected by the phase detector and Fl divided by N becomes equal to F2 (10 khz) when the phase locked loop is under locked condition.

Therefore Fvco is determined by the following formula, relating Fstd and the divide ratio N.

$$Fvco = Fstd + 10 \times N$$

Fvco is changeable at the increment of 10 khz by varying the program divide ratio N. For example, the divide ratio N is programmed to 109 at channel No. 1, therefore Fvco is calculated as follows:

$$Fvco = 36{,}570 + 10 \times 109$$
$$= 36{,}570 + 1090 = 37{,}660 \text{ khz}$$

Note: refer to table A for remaining channels

Table B Divide Ratio N

Channel No.	Divide Ratio(N)	Program input level									
		1A	1B	1C	1D	2A	2B	2C	2D	3A	3B
1	109	H	L	L	H	L	L	L	L	H	L
2	110	L	L	L	L	H	L	L	L	H	L
3	111	H	L	L	L	H	L	L	L	H	L
4	113	H	H	L	L	H	L	L	L	H	L
5	114	L	L	H	L	H	L	L	L	H	L
6	115	H	L	H	L	H	L	L	L	H	L
7	116	L	H	H	L	H	L	L	L	H	L
8	118	L	L	L	H	H	L	L	L	H	L
9	119	H	L	L	H	H	L	L	L	H	L
10	120	L	L	L	L	L	H	L	L	H	L
11	121	H	L	L	L	L	H	L	L	H	L
12	123	H	H	L	L	L	H	L	L	H	L
13	124	L	L	H	L	L	H	L	L	H	L
14	125	H	L	H	L	L	H	L	L	H	L
15	126	L	H	H	L	L	H	L	L	H	L
16	128	L	L	L	H	L	H	L	L	H	L
17	129	H	L	L	H	L	H	L	L	H	L
18	130	L	L	L	L	H	H	L	L	H	L
19	131	H	L	L	L	H	H	L	L	H	L
20	133	H	H	L	L	H	H	L	L	H	L
21	134	L	L	H	L	H	H	L	L	H	L
22	135	H	L	H	L	H	H	L	L	H	L
23	138	L	L	L	H	H	H	L	L	H	L
24	136	L	H	H	L	H	H	L	L	H	L
25	137	H	H	H	L	H	H	L	L	H	L
26	139	H	L	L	H	H	H	L	L	H	L
27	140	L	L	L	L	L	L	H	L	H	L
28	141	H	L	L	L	L	L	H	L	H	L
29	142	L	H	L	L	L	L	H	L	H	L
30	143	H	H	L	L	L	L	H	L	H	L
31	144	L	L	H	L	L	L	H	L	H	L
32	145	H	L	H	L	L	L	H	L	H	L
33	146	L	H	H	L	L	L	H	L	H	L
34	147	H	H	H	L	L	L	H	L	H	L
35	148	L	L	L	H	L	L	H	L	H	L
36	149	H	L	L	H	L	L	H	L	H	L
37	150	L	L	L	L	H	L	H	L	H	L
38	151	H	L	L	L	H	L	H	L	H	L
39	152	L	H	L	L	H	L	H	L	H	L
40	153	H	H	L	L	H	L	H	L	H	L

1A is the least significant bit, and
3B is the most significant bit.
H : High level (more than 3.5 volts D.C.)
L : Low level (less than 1.0 volt D.C.)

Table A Frequency Chart of Fvco

Channel No.	Divide ratio(N)	Fl(MHz)	Fstd(MHz)	Fvco(MHz)
1	109	1.090	36.570	37.660
2	110	1.100	36.570	37.670
3	111	1.110	36.570	37.680
4	113	1.130	36.570	37.700
5	114	1.140	36.570	37.710
6	115	1.150	36.570	37.720
7	116	1.160	36.570	37.730
8	118	1.180	36.570	37.750
9	119	1.190	36.570	37.760
10	120	1.200	36.570	37.770
11	121	1.210	36.570	37.780
12	123	1.230	36.570	37.800
13	124	1.240	36.570	37.810
14	125	1.250	36.570	37.820
15	126	1.260	36.570	37.830
16	128	1.280	36.570	37.850
17	129	1.290	36.570	37.860
18	130	1.300	36.570	37.870
19	131	1.310	36.570	37.880
20	133	1.330	36.570	37.900
21	134	1.340	36.570	37.910
22	135	1.350	36.570	37.920
23	138	1.380	36.570	37.950
24	136	1.360	36.570	37.930
25	137	1.370	36.570	37.940
26	139	1.390	36.570	37.960
27	140	1.400	36.570	37.970
28	141	1.410	36.570	37.980
29	142	1.420	36.570	37.990
30	143	1.430	36.570	38.000
31	144	1.440	36.570	38.010
32	145	1.450	36.570	38.020
33	146	1.460	36.570	38.030
34	147	1.470	36.570	38.040
35	148	1.480	36.570	38.050
36	149	1.490	36.570	38.060
37	150	1.500	36.570	38.070
38	151	1.510	36.570	38.080
39	152	1.520	36.570	38.090
40	153	1.530	36.570	38.100

Channel Selection Program

The divide ratio of the programmable frequency divider in IC-3 is determined by the input voltage to the program input terminals, pin No. 13 through pin No. 22 of the IC. The program input voltage for pin No. 13 through pin No. 19 are supplied from the channel selector switch, S-306 and the input for pin No. 20 and 22 are fixed to "low level" and the input for pin No. 21 is fixed to "high level."

The funtion of the program input terminals is as follows:

Pin No.	13	14	15	16	17	18	19	20	21	22
Function	1A	1B	1C	1D	2A	2B	2C	2D	3A	3B
Significance Number	1	2	4	8	10	20	40	80	100	200

Note: Each program input is affected when the input voltage is in "high level."

The divide ratio N of the programable divider is given by the sum of the significance numbers which are affected by supplying a "high level" input. For example when the channel selector switch is set to channel No. 1, the input of 1A, 1D and 3A is in "high level" and the input of the other terminals is in "low level". Therefore divide ratio N is determined as follows:

$$N = 1 + 8 + 100 = 109$$

See table B for remaining channels.

ALIGNMENT OF TRANSMITTER PORTION

1. Test equipment required

   a. RF output power meter
   b. 50 ohm load and attenuator
   c. Oscilloscope (0 - 30MHz)
   d. Frequency Counter (o - 30MHZ)
   e. Audio Frequency signal generator
   f. Audio Frequency milli-volt meter
   g. Hamonics meter

2. Alignment procedure

STEP	PRESET	CONNECTIONS	ADJUSTMENT	REMARKS
1.	Transmitter mode, no modulation	Oscilloscope to the base of TR8 (TP 3)	L18	Adjust L18 for the maximum indication of carrier on oscilloscope
2.	Transmitter mode, no modulation	Oscilloscope to secondary of L17 (TP 3)	L17	Adjust L17 for the maximum indication
3.	Same as step 2	RF output power meter to ANT jack (J301)	L16 L15 L12	Adjust L16, L15 and L12 for the maximum indication on RF output power meter
4.	Same as step 2	Same as step 3	L18 L17 L16 L15 L12 L11	Adjust L18, L17, L16 L15, L12 and L11 for the maximum reading
5.	Same as step 2	Same as step 3	L12	Adjust L12 to obtain RF output power of 3.8 watt b y rotating the slug core clockwise
6.	Same as step 2	Same as step 3	VR4	Adjust VR4 for a proper indication on RF power meter
7.	Same as step 2	Harmonics meter ANT jack (J301)	L10	Adjust L10 for the minimum reading of 2nd harmonics

STEP	PRESET TO	CONNECTIONS	ADJUSTMENT	REMARKS
8	Transmitter mode, no modulation	Frequency counter to ANT. jack (J301) thru a suitable load and attenuator		Check frequency of all channels
9	Transmitter mode, channel 19 AF input of 1,000 Hz 10mV to mike jack	Oscilloscope to ANT. Jack thru a suitable load and attenuator AF generator to mike jack (J401)	VR5	Adjust VR5 to obtain 95% modulation
10	Same as step 9	Same as step 9	VR6	Adjust VR6 for indication of modulation percentage properly

ALIGNMENT OF RECEIVER PORTION

1. Test equipment required

   a. Signal generator (455 KHz and 27 MHz band, 1,000 Hz 30% amplitude modulation and 50 ohm output impedance)
   b. AF output meter
   c. Oscilloscope (AF)
   d. Dummy load (8 ohm, 10 watt, resistive)

2. Alignment procedure

STEP	PRESET TO	CONNECTIONS		ADJUSTMENT	REMARKS
		SIGNAL GENERATOR	OUTPUT METER		
1	ANL:OFF SQL: Min. VOL:Max	To base of TR3 thru 0.01uF Cap. Freq.: 455 KHz	To EXT. SPKR Jack (J304)	L6, L7, L8	Adjust L6, L7 and L8 for the maximum AF output
2	Same as step 1, Channel 19	To Ant. connector (J301) Freq: 27.185MHz	Same as step 1	L1, L2, L3, L4	Adjust L1, L2, L3 and L4 for the Maximum AF output
3	Same as step 2	Same as step 2 and Output: 0.9uV	Same as step 1	VR2	Adjust VR2 to obtain 2V AF output
4	ANL:OFF SQL:Max. VOL:Max. Channel 19	Same as step 2 and output 500 uV	Same as step 1	VR3	Adjust VR3 to obtain 2V AF output
5	Same as Step 2	Same as step 2 and Output: 100uV	Same as step 1	VR1	Adjust VR1 to obtain "S 9" indication on "S" meter
6	Repeat the above adjustments, in order to confirm if the adjustments were made correctly.				

ALIGNMENT OF NOISE BLANKER PORTION

1. Test equipments required

   a. Signal generator (23.5MHz, 50 ohm output impedance)
   b. RF VTVM

2. Alignment procedure

Step	CONNECTIONS		ADJUSTMENT	REMARKS
1	Signal generator to ANT. jack (J301) at frequency of 23.5MHz	RF VTVM to base of TR26(TP 7)	L27	Adjust L27 for the maximum reading on RF VTVM (Do not adjust L28)

29XLR

FUNCTION OF SEMICONDUCTORS

Transistors

TR-1	RF amp (RV)
TR-2	1st mixer (RV)
TR-3	2nd mixer (RV)
TR-4	IF amp
TR-5	IF amp
TR-6	Final (TX)
TR-7	Driver (TX)
TR-8	Buffer (TX)
TR-9	Mixer (TX)
TR-10	Osc. (TX)
TR-11	Audio Pre-Amp
TR-12	Squelch Gate
TR-13	Squelch Amp
TR-14	Limiter Amp
TR-15	Limiter Amp
TR-16	Limiter Amp
TR-17	Instant Stop
TR-18	PLL Mixer
TR-19	PLL Local Osc.
TR-20	Mode Switching
TR-21	Delta Tune Switching
TR-23	Mod. Ind. Amp
TR-25	DC amp
TR-26	NB Pulse amp
TR-27	NB Pulse amp
TR-28	NB Pulse amp

ICs

IC-1	Audio amp
IC-2	Mike amp
IC-3	PLL
IC-4	PLL interface
IC-5	PLL VCO
IC-6	Regulator
IC-7	Noise amp

Diodes

D-1	Protector (RV)
D-2	Protector (RV)
D-3	Protector (RV)
D-4	Detector (RV)
D-5	S Meter detector
D-6	ANL Gate
D-7	Switching diode
D-8	SWR detector
D-9	SWR detector
D-10	Switching diode
D-11	Modulation stabilizer
D-12	Modulation limiter
D-13	Modulation limiter
D-14	AMC Detector
D-15	Delta tune control
D-16	Switching diode
D-17	Voltage stabilizer
D-18	Voltage stabilizer
D-19	Polarity protector
D-20	Noise amp protector
D-21	Noise amp protector
D-22	Modulation detector
D-24	Bias
D-301	Channel Ind.
D-302	Modulation ind.

PC-198 (MAIN)

29XLR

IC7 uPC577H TR26 2SC458 TR27 2SA844 TR28 2SC458

MICROPHONE

VOLTAGE (V) SHOWN WITH ( ) ARE TX MODE AND WITHOUT ( ) SHOWS RX MODE

NOTES
1 ALL RESISTORS IN Ω 1/8W UNLESS OTHERWISE NOTED.
2 ALL CAPACITORS IN uF UNLESS OTHERWISE NOTED.

* SUBJECT TO CHANGE WITHOUT NOTICE.

TR1 2SC1342 TR2 2SK55 TR3 2SC460 TR4 2SC460 TR5 2SC460

TR6 2SC2092 TR7 2SC2091 TR8 2SC2076 TR9 3SK45 TR10 2SC460

TR12 2SK55 TR13 2SC458

IC1 uPC1156H

TR19 2SC460

IC5 uHIC004

TR18 3SK45B09

IC6 78L05

TR11 2SC458

IC2 uPC592H2

TR17 2SC458

TR14 2SC458

TR21 2SC458 TR25 2SD467

TR23 2SC458

TR15 2SA844 TR16 2SC458

TR20 2SA673

IC3 uPD858C

IC4 4011

M301 METER

S/RF SWR

RF GAIN J301 ANT

S303a S/RF CAL

S303b S/RF CAL

S3014 NB ANL OFF

S3018 NB ANL OFF

S307 HI CUT

VR301 50K A VOLUME

VR302 20K B SQUELCH

VR303 50K B MIC GAIN

VR304 50K B

VR305 20K B DELTA TUNE

VR306 10KB DIMMER

S3048 PA CB

S305 POWER

S306 ROTARY CHANNEL SELECTOR

PC-207 (CH)

PC-181

J401 MIKE

J303 PA

J304 EXT SP

J306 DC CONN

SP301 SPEAKER

D301 TLR321

D302 LRO702R MOD

L301 LD072

L302 YY045

L303 LD080

L304 LD012

L307 LD080

L308 LD080

L309 LD080

T1 TF107

T2 TF017

F1 2A

DC 13-8V

TO S305

TO S304

TO S304B

TO VR301

5V COM

GND

UFP

LED COM