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NJ88C28

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

(Supersedes version in May 1992 Personal Communications IC Handbook)

The NJ88C28 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C28 is intended to be used in conjunction with a two-modulus prescaler such as the SP8715 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- 5V Operation
- Fast Lock Up Time
- SSOP Package Option

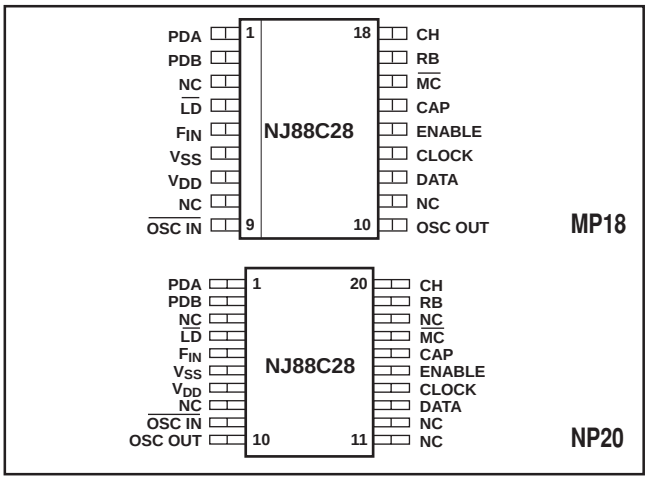


Fig.1 Pin connections - top view (not to scale)

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	–0·75V to 7V
Input voltage	
Open drain output, pin 4	7V
All other pins	V_{SS} – 0·3V to V_{DD} + 0·3V
Storage temperature	–55°C to +125°C

ORDERING INFORMATION

NJ88C28 IG MPES Miniature Plastic DIL Package
NJ88C28 IG NPAS Shrunk Miniature Plastic DIL Package

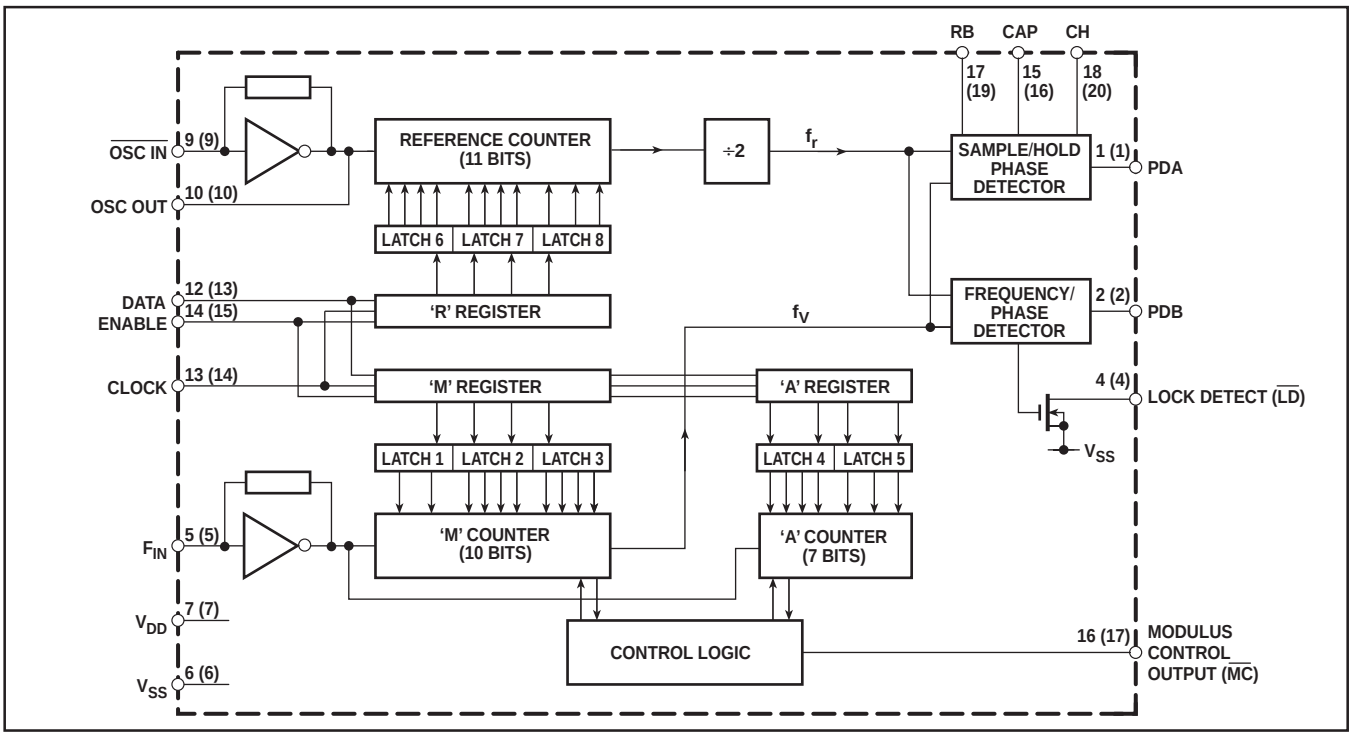


Fig.2 Block diagram (NP pinout shown in brackets)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions, unless otherwise stated:

V_{DD}–V_{SS} = 5V ±0·5V. Temperature range = – 40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5·3	7·0	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
		0.9	1·4	mA	f_{osc}, f_{FIN} = 4·096MHz } 0 to 5V square wave
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7·0	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±100	nA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, F_{IN} and $\overline{OSCIN}$ inputs	20			MHz	Input squarewave V_{DD} to V_{SS}, 25°C. See note 5.
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			µs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0·5			µs	
Enable set-up time, t_{ES}	0·2		t_{CH}	µs	
Enable hold time, t_{EH}	0·2			µs	
Data set-up time, t_{DS}	0·2			µs	
Data hold time, t_{DH}	0·2			µs	
Clock rise and fall times			0·2	µs	
High level threshold			V_{DD}–0·8	V	See note 1
Low level threshold	0·8			V	See note 1
Hysteresis	1·0	2·0		V	See note 1
Phase Detector					See note 3
Positive going threshold, V_T+		V_{DD}–1·25		V	
Negative going threshold, V_T–		V_{SS}+1·05		V	
Digital phase detector propagation delay		500		ns	
RB current, I_{RB}	1		600	µA	Set by external conditions.
CAP/RB current gain, α	6·9	7·8	9·0		Over RB current range.
Programming capacitor, CAP		53		pF	C_{int} plus packaging strays.
Output resistance, PDA, PDB		80		Ω	

NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers with typical thresholds of V_{SS}+0·8V and V_{DD}–0·8V. These inputs do not have pull-up resistors and are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically; 1µs for the sample and hold amplifier.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.
5. The CAP reset device limits the minimum f_{in} period due to its time constant formed by the CAP pin's capacitance value. A typical $R_{DS(ON)}$ is about 1kΩ. Refer to AN112 for further details.

PIN DESCRIPTIONS

Pin no. NP	Pin no. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as f_v (the output from the 'M' counter) phase lead increases; voltage decreases as f_r (the output from the 'R' counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). This pin is at $(V_{DD}–V_{SS})/2$ when the system is in lock, for an external loop filter amplifier biased to $(V_{DD}–V_{SS})/2$. Ideally, V_{BIAS} should be chosen such that the PDA window is centred between the thresholds, typically at $0{\cdot}55(V_{DD}–V_{SS})$
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance. (Minimum, $M = 3$ for correct function of PDB).
3	3	NC	Not connected.
4	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	5	F_{IN}	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	6	V_{SS}	Negative supply (ground).
7	7	V_{DD}	Positive supply.
8	8	NC	Not connected.
9,10	9,10	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 2·2kΩ resistor between pin 10 and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the total division ratio being twice the programmed value i.e., 6 to 4094 in steps of 2.
11	11	NC	Not connected.
12	–	NC	Not connected.
13	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C28; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
14	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
15	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
16	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
17	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 3-1023 but M ≥8 for correct PDA operation and, for correct operation with a prescaler, $M \geq A$. Where every possible channel is required, the minimum total division ratio N should be: $N \geq P^2 – P$, where $N = MP+A$.
18	–	NC	Not connected

Continued...

PIN DESCRIPTIONS (continued)

Pin no.		Name	Description
NP	MP		
19	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}. I_{RB} <600µA at V_{DD} = 5V.
20	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,
fcomp = comparison frequency,
R = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12·5kHz is required,

$$R = \frac{10^7}{2 \times 12{\cdot}5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2×400 = 800 since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P/P+1*)and the comparison frequency.

The division ratio $N = MP+A$,
where *M* is the ratio of the 'M' counter in the range 3 to 1023 and *A* is the ratio of the 'A' counter in the range 1 to 127.

Note that $M \geq A$ and

$$N = \frac{f_{VCO}}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12·5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12{\cdot}5 \times 10^3} = 22 \times 10^3$$

Now, $N = MP+A$, which can be rearranged as $N/P = M + A/P$. In our example we have $P = 64$, therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that $M = 343$ and $A/64 = 0.75$.

Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part×64 i.e., $A = 0{\cdot}75 \times 64 = 48$.
NB The minimum ratio *N* that can be used is $P^2 - P$ (4032 in our example) for all contiguous channels to be available.

To check: $N = 343 \times 64 + 48 = 22000$, which is the required division ratio and is greater than 4032 ($= P^2 - P$).

When re-programming, the counters are changed only at the zero state. There is no reset to zero, which means that the synthesiser loop lock up time will be variable with respect to the programming sequence timing. When only small changes in frequency are required, the NJ88C28 non-resettable synthesiser should achieve the shortest loop lock up times.

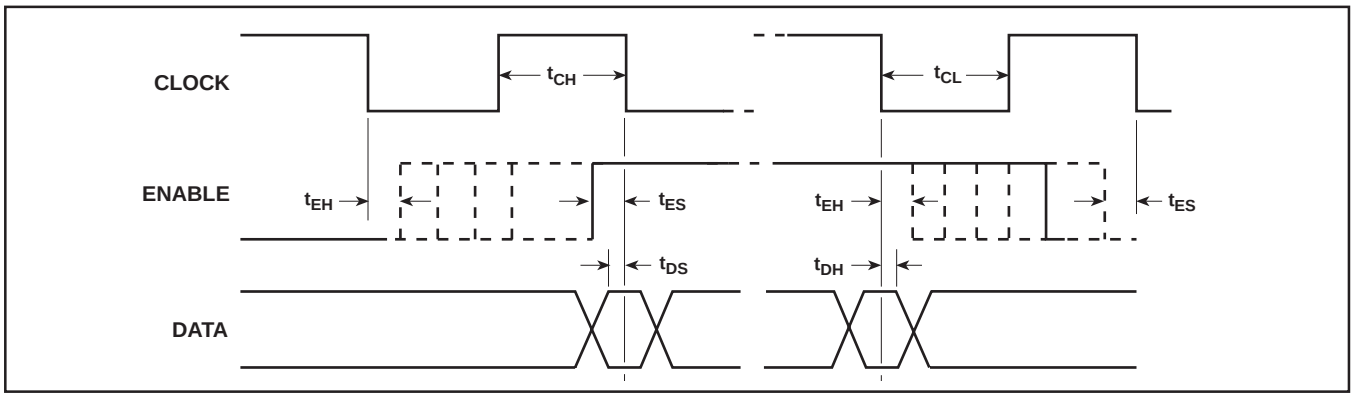


Fig. 3 Timing diagram showing timing periods required for correct operation

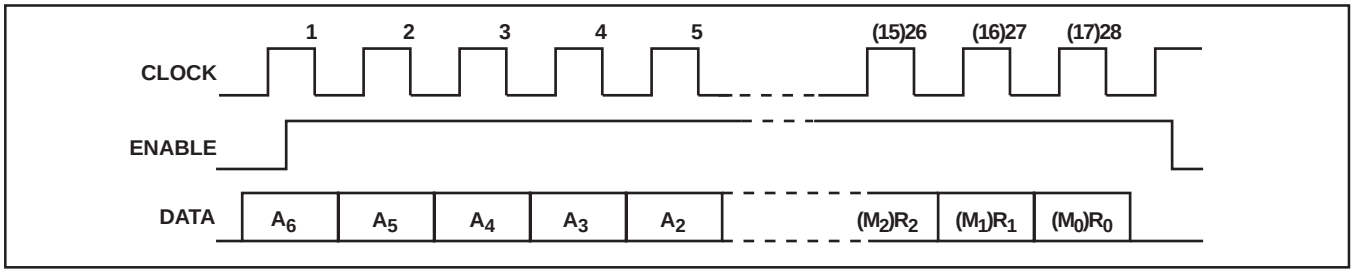


Fig. 4 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD}\,K_{VCO}}{N}$$

where K_{PD} is the phase detector constant (volts/rad), K_{VCO} is the VCO constant (rad/sec-volt) and N is the overall loop division ratio. When N is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C28 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at the bias voltage set by the external loop filter amplifier; any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain, K_{PDA}, which is programmable with an external resistor, RB, and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator. Typically, the gain is given by:

$$K_{PDA} = \frac{\alpha I_{RB}}{2\pi\, C_{CAP}\, f_{comp}}$$

where C_{CAP} = internal 50pF $\bar{}$ C_{EXT}. Application Note AN112 deals with this further.

A hold capacitor (CH) of non-critical value, which might be typically 470pF, is connected from pin 18 to V_{SS}. A smaller value is sufficient if the required sideband performance is not high. The output from the sample and hold phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO. The PDB gain is:

$$K_{PDB} = \frac{V_{DD}}{4\pi}$$

The stated minimum of 3 for the 'M' counter is true for the PDB output only. To avoid race conditions in the internal phase comparator counter for controlling the PDA timing, the minimum division ratio for the 'M' counter should be 8 or more. Fig. 6 shows a typical NJ88C28 application.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 10 (OSC OUT) and the other components, as shown in Fig. 5. A value of between 220Ω and 2·2kΩ is advised, depending on the crystal series resistance.

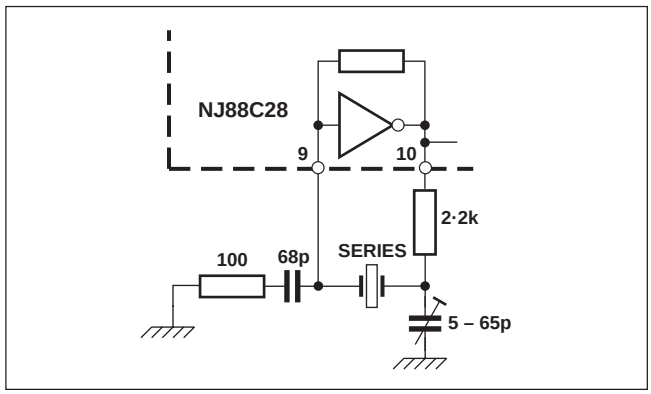


Fig. 5 Suggested crystal oscillator circuit

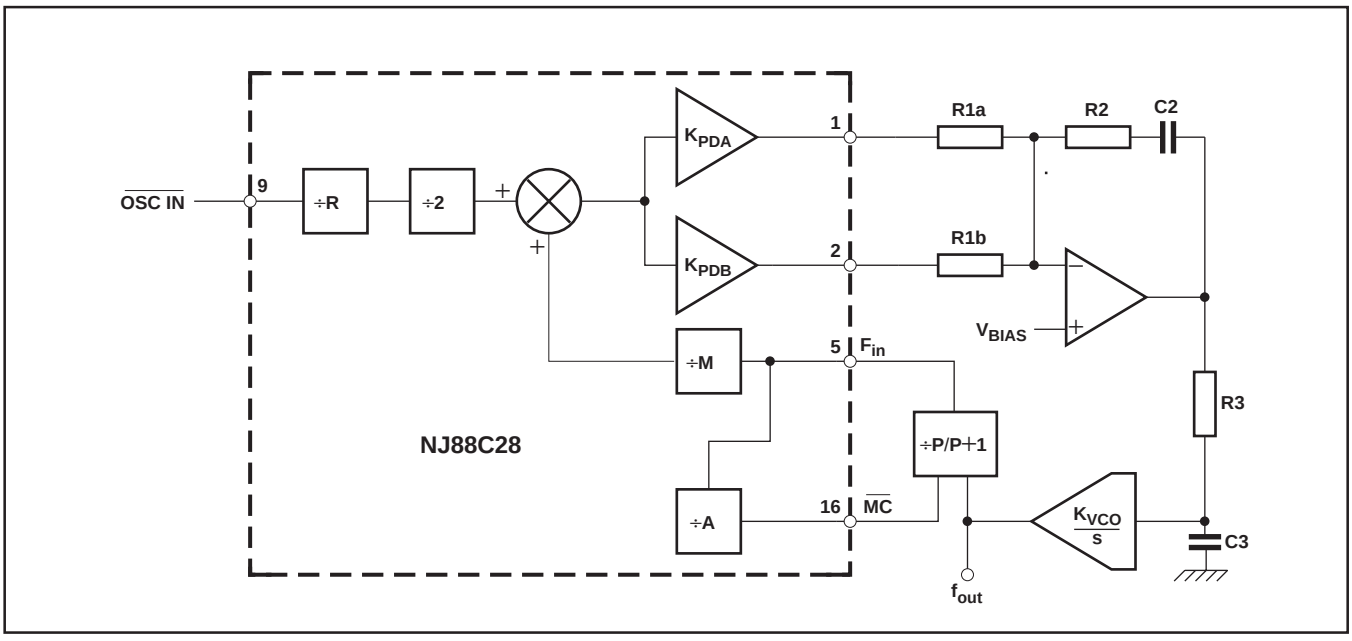


Fig.6 NJ88C28 application circuit

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur. When programming the device, DATA, ENABLE and CLOCK pins must not exceed V_{DD} as lock up times may be compromised. A suggested interface to prevent this situation is shown in Fig. 7.

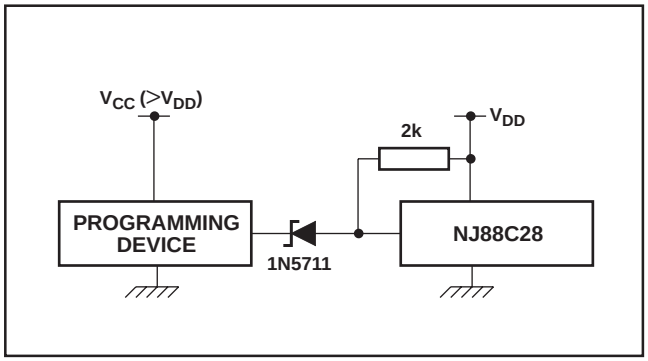


Fig. 7 Suggested programming circuit

LOOP EQUATIONS

$$\omega_0 = \left[\frac{K_{VCO} K_{PD}}{N \mathbf{R} C_2 C_3 R_3} \right]^{\frac{1}{3}}$$

$$\zeta = [\Sigma K_{VCO} K_{PD} R_2 \Pi / \{\Sigma N C_3 R_3 \varphi_0{}^2 \Pi - 1\} \partial / 2\mathbf{R}$$

$$C_3 R_3 = \equiv \varphi_0 \Sigma 2\zeta + \mathbf{R} \Pi \partial^{-1}$$

$$R_2 = \frac{N \varphi_0 \Sigma 1 + 2\zeta \mathbf{R} \Pi}{K_{VCO} K_{PD} \Sigma \mathbf{R} + 2\zeta \Pi}$$

$$C_2 = \frac{K_{VCO} K_{PD} \Sigma 2\zeta + \mathbf{R} \Pi}{N \mathbf{R} \omega_0{}^2}$$

where ω_0 = loop natural frequency
ζ = damping factor
$\mathbf{R}$ = ratio of real pole to ω_0
$N = MP + A$
$K_{PD} = K_{PDA} / R_{1a}$
or $K_{PD} = K_{PDB} / R_{1b}$
provided $R_{1a} \gg R_{1b}$

$$\text{PDA window} = \frac{V_{DD} - \equiv \Sigma V_{T+} \Pi + \Sigma V_{T-} \Pi \partial N f_{comp}}{2\pi K_{PDA}}$$

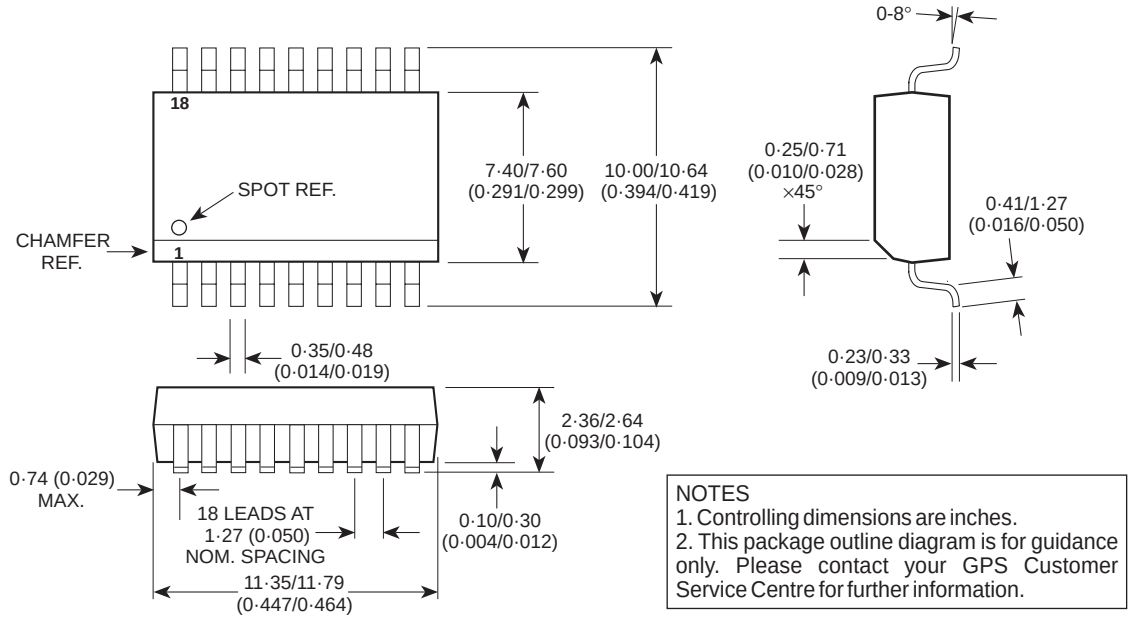
Further details are to be found in Application Note AN112.

NOTES

NJ88C28

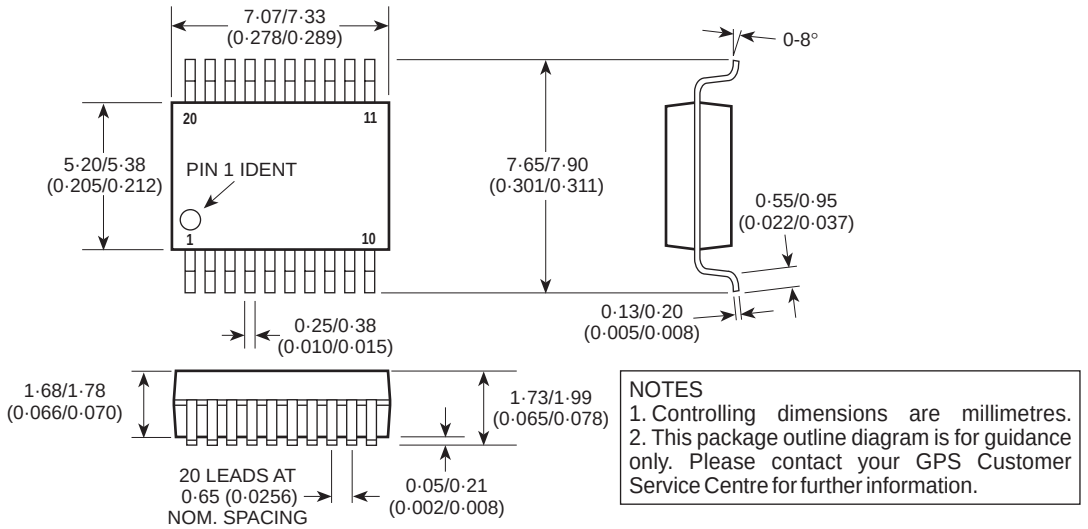
PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

18-LEAD MINIATURE PLASTIC DIL - MP18



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

20-LEAD SHRUNK MINIATURE PLASTIC DIL (SSOP) - NP20

GEC PLESSEY
SEMICONDUCTORS

HEADQUARTERS OPERATIONS
GEC PLESSEY SEMICONDUCTORS
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (01793) 518000
Fax: (01793) 518411

GEC PLESSEY SEMICONDUCTORS
P.O. Box 660017
1500 Green Hills Road,
Scotts Valley, CA95067-0017
United States of America.
Tel (408) 438 2900
Fax: (408) 438 5576

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