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GEC PLESSEY
SEMICONDUCTORS

DS3280-1.3

NJ88C25

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered Band 0 and Band 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 30 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 19 bits, when only the 'A', 'M' and 'B' counters require changing.

The NJ88C25 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

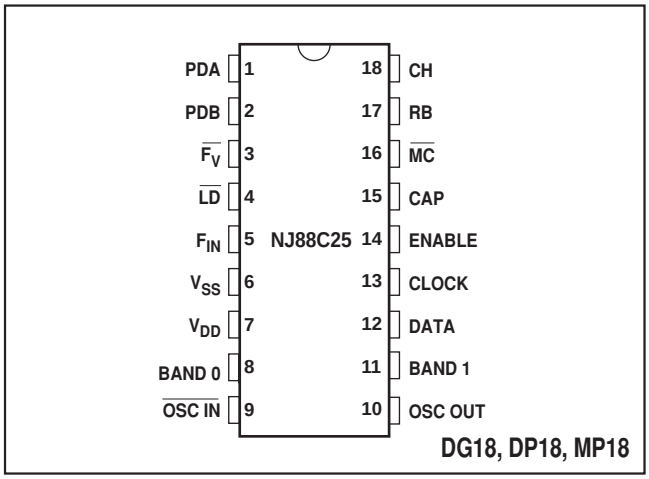

Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature

ORDERING INFORMATION

NJ88C25 KA DG Ceramic DIL Package
NJ88C25 KA DP Plastic DIL Package
NJ88C25 KA MP Miniature Plastic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$: −0·5V to 7V
Input voltage
Open drain output, pins 3 and 4: 7V
All other pins: $V_{SS}-0{\cdot}3V$ to $V_{DD}+0{\cdot}3V$
Storage temperature: −65°C to +150°C (DG package)
−55°C to +125°C
(DP and MP packages)

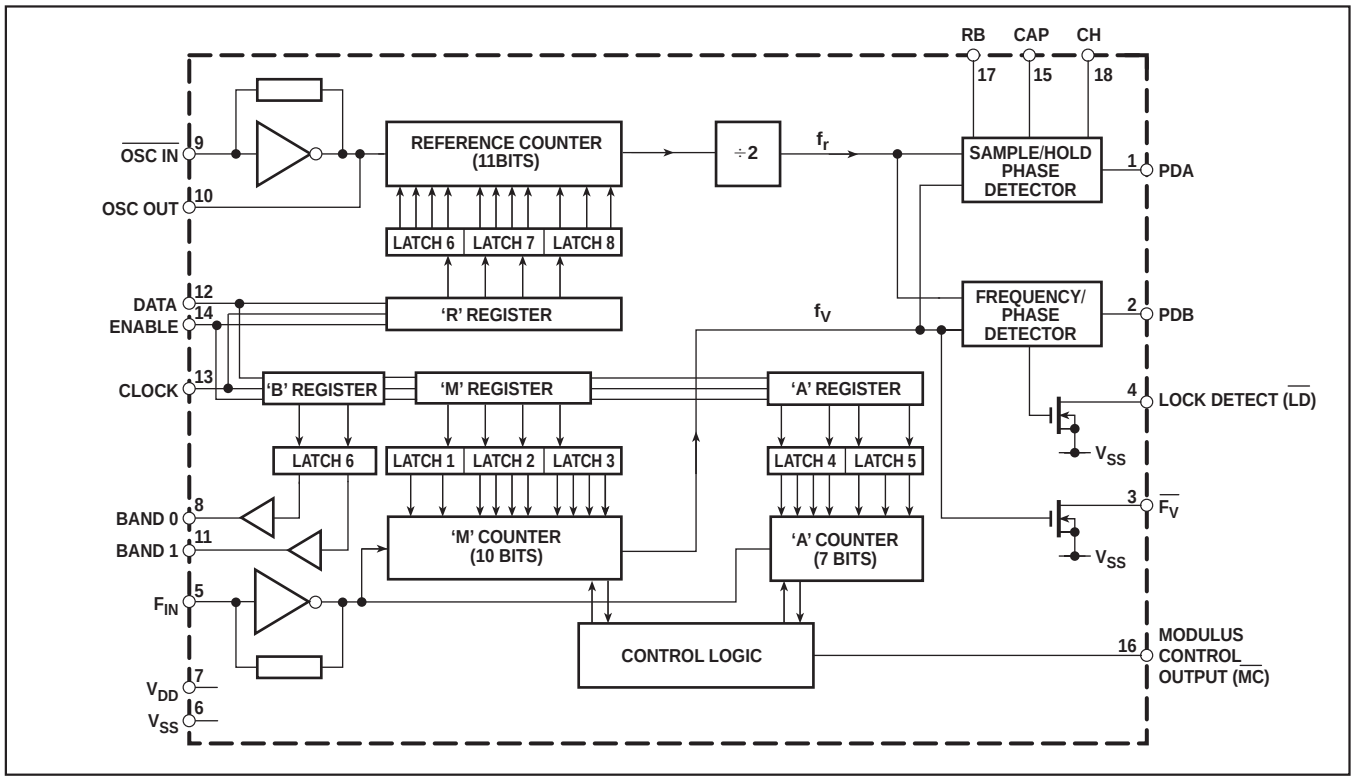

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=2·7V to 5·5V. Temperature range = –30°C to +70°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5·5		mA	f_{osc}, f_{FIN} = 20MHz } 0 to 5V square wave
		0·7		mA	f_{osc}, f_{FIN} = 1MHz } 0 to 5V square wave
		3·7		mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
OUTPUTS					
Modulus Control ($\overline{MC}$), BAND 1 and BAND 2					
High level	V_{DD}−0·4			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect ($\overline{LD}$) and $\overline{F_V}$					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7·0	V	
PDB					
High level	4·6			V	I_{SOURCE} = 4mA
Low level			0·4	V	I_{SINK} = 4mA
3-state leakage current			±0·1	µA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	20			MHz	Input squarewave V_{DD} to V_{SS},
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			µs	All timing periods are referenced to the negative transition of the clock waveform. See note 5
Clock low time, t_{CL}	0·5			µs	
Enable set-up time, t_{ES} (see note 5)	0·2		t_{CH}	µs	
Enable hold time, t_{EH}	0·2			µs	
Data set-up time, t_{DS}	0·2			µs	
Data hold time, t_{DH}	0·2			µs	
Clock rise and fall times	0·2			µs	
Positive threshold	3			V	TTL compatible, see note 1
Negative threshold			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	See note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the $\overline{OSC\ IN}$ and F_{IN} inputs.
5. Clock to enable set-up time (t_{ES}) is variable, dependent on f_{OSC}. It needs to be specified in terms of f_{OSC}, clock high time (t_{CH}) and clock low time (t_{CL}) and must meet the following conditions: $4\times1/f_{OSC} \leqslant t_{ES} < (t_{CH}+t_{CL})$.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as f_v (the output from the 'M' counter) phase lead increases; voltage decreases as f_r (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{F_V}$	This pin is an open drain output from the 'M' counter.
4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	F_{IN}	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	V_{SS}	Negative supply (ground).
7	V_{DD}	Positive supply (normally 5V)
9,10	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between OSC $\overline{OUT}$ and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 , with the total division ratio being twice the programmed number.
8, 11	BAND 0/1	Two latch outputs, providing an output of the data from the 'B' register.
12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are four data words which control the NJ88C25; MSB is first in the order: 'A' (7 bits), 'M' (10 bits),]B' (2 bits) and 'R' (11 bits).
13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 30 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'B','M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'B', 'M' and 'A' have been loaded. If 30 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geqslant A$. Where every possible channel is required, the minimum total division ratio N should be: $N \geqslant P^2 - P$.
17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

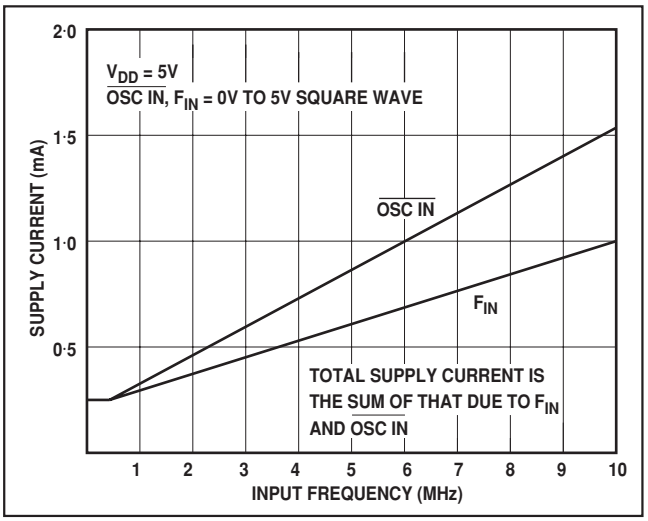

Fig. 3 Typical supply current v. input frequency

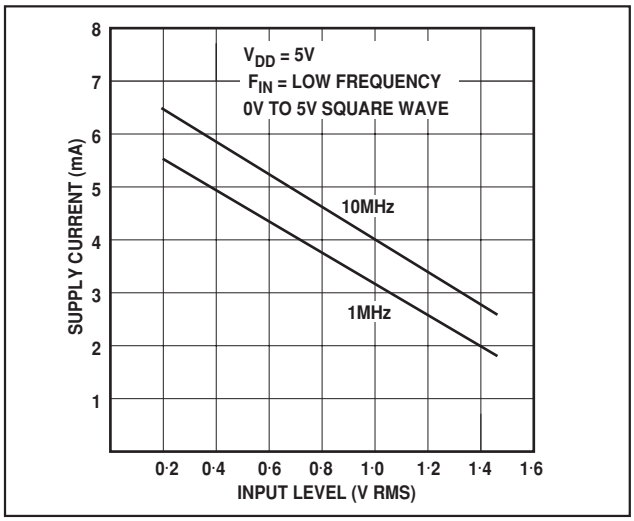

Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of th 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,
fcomp = comparison frequency,
R = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12·5kHz is required,

$$R = \frac{10^7}{2 \times 12{\cdot}5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2×400 = 800 since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P/P+1*)and the comparison frequency .

The division ratio $N = MP + A$,
where *M* is the ratio of the 'M' counter in the range 8 to 1023 and *A* is the ratio of the 'A' counter in the range 0 to 127. Note that $M \geqslant A$ and

$$N = \frac{f_{VCO}}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12·5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12{\cdot}5 \times 10^3} = 22 \times 10^3$$

Now, $N = MP + A$, which can be rearranged as $N/P = M + A/P$. In our example we have $P = 64$, therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that $M = 343$ and $A/64 = 0{\cdot}75$.
Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part×64 i.e., $A = 0{\cdot}75 \times 64 = 48$.
NB The minimum ratio *N* that can be used is $P^2 - P$ (=4032 in our example) for all contiguous channels to be available.

To check: $N = 343 \times 64 + 48 = 22000$, which is the required division ratio and is greater than 4032 ($= P^2 - P$).

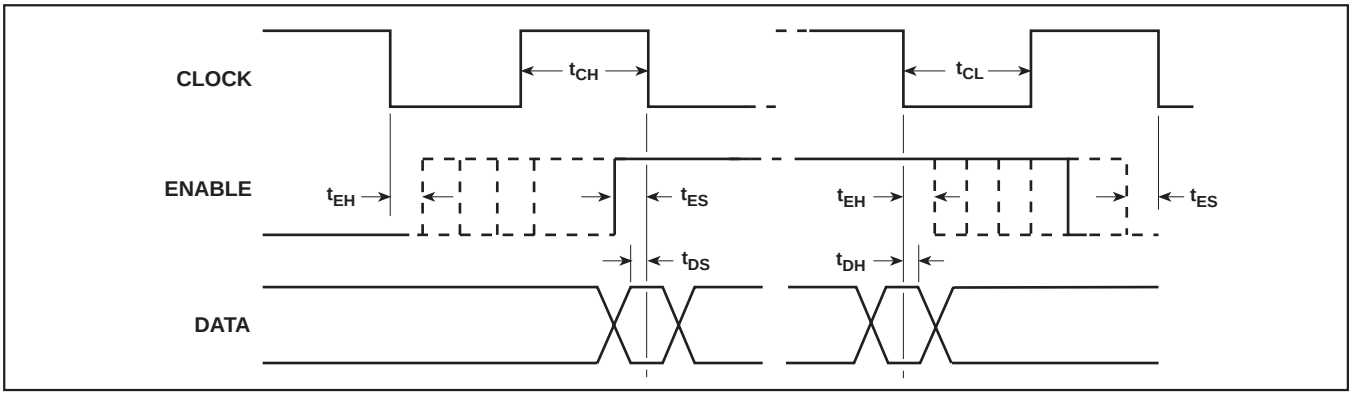

Fig. 5 Timing diagram showing timing periods required for correct operation

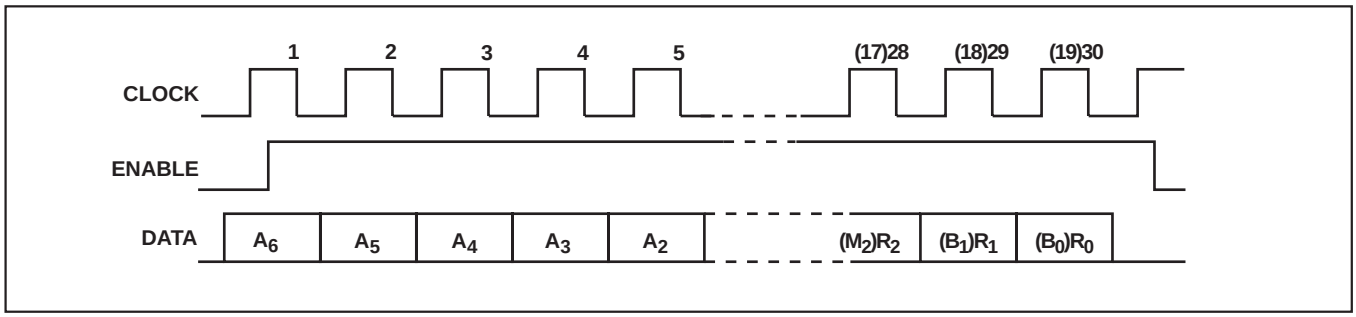

Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD}\,K_{VCO}}{N}$$

where K_{PD} is the phase detector constant (volts/rad), K_{VCO} is the VCO constant (rad/sec/volt) and N is the overall loop division ratio. When N is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C25 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output,PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain, K_{PDA}, which is programmable with an external resistor, RB, and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator.

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